

Notice of References Cited	Application/Control No. 10/643,193		Applicant(s)/Patent Under Reexamination BHAVNAGARWALA ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,731,916	05-2004	Haruyama	455/194.2
	B	US-4,851,768	07-1989	Yoshizawa et al.	324/751
	C	US-6,181,621	01-2001	Lovett	365/205
	D	US-6,628,146	09-2003	Tam	327/63
	E	US-6,161,213	12-2000	Lofstrom	716/4
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Bastos et al., "Mismatch characterization of small size MOS transistors", Proceedings of the IEEE 1995 Int. Conference on Microelectronic Test Structures, Vol. 8, March 1995.			
	V	Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime", Proceedings of the IEEE 1997 Int Conference on Microelectronic Test Structures, Vol. 10, March 1997.			
	W	Lakshmikumar et al., "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design", IEEE Journal of Solid-State Circuits, Vol. 21, Issue: 6, Dec 1986.			
	X	Pavasovic et al., "Characterization of Subthreshold MOS Mismatch in Transistors for VLSI Systems", Journal of VLSI Signal Processing, 8, 75-85, 1994.			

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	G	US-			
	H	US-			
	I	US-			
	J	US-			
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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Bhavnagarwala et al., "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability", IEEE Journal of Solid-State Circuits, Vol. 36, No. 4, April 2001.
	V	
	W	
	X	

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.